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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,933	WU ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-20,22-39,52-58,61-65,76,77 and 91-110* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-20, 22-39,52-58,61-65,76,77, 91-110* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/02/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7,9-20, 22-39,52-58,61-65,76,77 and 91-98 were previously examined.

2. Claims 99-104 were added.

3. Claims 1-7,9-20, 22-39,52-58,61-65,76,77, 91-110 were examined.

Section I: Non-Final Rejection

Claim Rejections - 35 USC § 103

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a

person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-7,9-20, 22-39,52-58,61-65,76,77, 91-110 are rejected under 35 U.S.C. 103 (a) as being unpatented over Chen et al.,titled,"A Unified Compact Scalable Model for Hot Carrier Reliability Simulation" (hereafter Chen) in view of Kadoch et al. (US Patent 5,761,481;hereafter Kadoch), and in further view of Rajgopal et al. (US Patent 6,363,515,hereafter Rajgopal)

Regarding claims 1,6,37,38,57,58,61,76,91-95,97-110

Chen teaches

- simulating (Chen: introduction, 2nd paragraph, line 7)
- degradation of a circuit (Chen: "MOSFET degradation", introduction, 1st sentence),
- circuit stress time (Chen: pg. 246, figure 5, plurality of stress times)

- a plurality of values (Chen: pg. 246, figure 5, a plurality of different stress times
- supplying aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter").
- information on selected ones of the components; simulating behavior (Chen: pg.245, right column, lines 13 and 14)
- the circuit when fresh (Chen: pg.243, left column, 2nd paragraph, lines 9-10)
- a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6)
- relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times)
- using their respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter")
- determining the degraded operation (Chen: pg. 243, left column 2nd paragraph, line 6)
- information and respective relative component degradation parameter at the plurality supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) values

Chen fails to simulate a circuit on a single run, netlist and specified components

Rajgopal teaches

- providing a netlist (Rajgopal: column 5, line 63)

Kadoch teaches

- simulating in a single run (Kadoch: column 2, line 62)

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the functional blocks of Rajgopal and the single run simulation of Kadoch in the circuit degradation simulation of Chen because Rajgopal teaches a need for a power estimation tool which makes it easier for the designer to determine the power usage of the system (Rajgopal: column 2, lines 2-4). Kadoch teaches a method to optimize fabrication process parameters needed in achieving desired electrical properties of the structure (Kadoch: column 2, lines 42-44).

Regarding claims 2

Chen teaches

- degradation of the circuit is due to hot-carrier effects (Chen: title).

Regarding claim 3

Chen teaches

- simulating is performed using a SPICE (Chen: Introduction, left column, 2nd paragraph) type circuit simulator.

Regarding claim 4

Chen teaches

- timing simulation (Chen: pg.246, figure 5, "stress time") type circuit simulator.
- aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information on

Regarding claim 5

Rajgopal teaches

- the selected ones of the components (Rajgopal: column 8, lines 40-42) is derived from electrical test data.

Regarding claim 6

Chen teaches

- simulating the behavior (Chen: pg.245, right column, lines 13 and 14)
- of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10) determines the waveforms at the nodes (Chen: pg.247, figure 10 response from fresh circuit model)

Regarding Claim 7

Chen teaches

- the supplied circuit age (Chen: pg. 244, equation 2 with right column, lines 4-8) parameters.

Regarding claim 9, 20,22,36

Rajgopal teaches

- distinct sets of components; first and second sets of components(Rajgopal: column 7, line 21).
- (Rajgopal: column 8, lines 40-42) each form different functional blocks

Regarding claims 10,23,25

Rajgopal teaches

- wherein a first of said sets of components (Rajgopal: column 8, lines 40-42) is an analog block and a second of said sets of components (Rajgopal: column 8, lines 40-42) is a digital block.

Regarding claims 11,26

Kadoch teaches

- performance criterion of the first set is transconductance (Kadoch: column 1, line 34)

Chen teaches

- the performance criterion of the second set is drain (Chen: pg.244, line 5) to source current.

Regarding claims 12,13,27,28,30

Rajgopal teaches

- the distinct sets of components (Rajgopal: column 8, lines 40-42) consist of different device types (resistors, capacitors, transistors, etc.).

- first of said different device types Rajgopal: column 8, lines 40-42) is an NMOS and a second of said different device types is a PMOS (MOSFETS cover NMOS and PMOS, well known).

Regarding claim 14,

Kadoch teaches

- the PMOS (MOSFETS cover NMOS and PMOS, well-known) performance criterion is leakage current (Kadoch: column 1, line 34).

Regarding claim 15,31

Chen teaches,

- the NMOS performance criterion is driving capability (Chen: pg.243, right column, 3rd paragraph, "forward/reverse operation" of degradation device)).

Regarding claim 16,32

Chen teaches

- a first of said different device types is a MOSFET (Chen: pg. 243, Introduction, left column, 1st paragraph) and a second of said different device types is a bipolar junction Transistor (i.e., JFETs well-known).

Regarding claim 17,29,33,62

Kadoch teaches

- the bipolar junction transistor performance criterion is leakage current (Kadoch: column 1, line 34).
- time dependence of a substrate current.(relates to the bipolar junction transistor, Kadoch: column 1, line 34)

Regarding claims 18,19,34

- wherein the distinct sets of components (Rajgopal: column 8, lines 40-42) employ different models for simulating a device that is the same.

Regarding claims 24, 54, 61

Chen teaches,

- the specified degradation level is expressed in terms of drain (Chen: pg.244, line 5).

Regarding claim 35

Rajgopal teaches,

- the first and second sets of components (Rajgopal: column 8, lines 40-42) each consist of a device type that is the same.

Regarding claims 39 and 56

Chen teaches,

- expressed in terms of lifetime (Chen: pg.244, line 7).

Regarding claims 52, 53,54,55,7695

Rajgopal teaches

- MOSFETs (Rajgopal: pg. 301, left column, 3rd paragraph).

Chen teaches

- to hot carrier effects (Chen: title).
- non-aged ("Fresh" Chen, pg. 247, figure 11) version.
- independent current sources, (Chen: pg. 246, figure 5) said determining comprising: supplying a physical model of the current magnitude (Chen: pg. 246, figure 5);
- establishing values of coefficients (Chen: pg. 246, equation 7, coefficients "A, B, C") in the physical model from electrical test data.

Regarding claim 63,

Chen teaches,

- a gate current (Chen: pg. 244, right column "Gate Bias Dependency").

Regarding claims 64,65,76,77, 91,97

Chen teaches

- the behavior (Chen: pg.245, right column, lines 13 and 14)
- a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6)
- relative to circuit age (Chen: pg. 244, equation 2 with right column, lines 4-8) comprises: simulating the behavior (Chen: pg.245, right column, lines 13 and 14) of the fresh circuit (Chen: pg.243, left column, 2nd paragraph, lines 9-10)
- an intermediate component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit stress time (Chen: pg. 246, figure 5, plurality of stress times);
- determining the degraded operation of the circuit at an intermediate circuit stress time (Chen: pg. 246, figure 5, plurality of stress times)
- using the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative intermediate component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6)at the

intermediate circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) value;

- of the degraded circuit at the intermediate circuit stress time (Chen: pg. 246, figure 5, plurality of stress times)
- a component degradation parameter (Chen: pg. 243, left column 2nd paragraph, line 6) relative to circuit age, (Chen: pg. 244, equation 2 with right column, lines 4-8) wherein
- the intermediate circuit stress time (Chen: pg. 246, figure 5, plurality of stress times)
- value is less than one of the circuit stress time (Chen: pg. 246, figure 5, plurality of stress times)
- values (Chen: pg. 246, figure 5, a plurality of different stress times).
- distinct quantized (age times as stated in spec. pg.6, lines 19-26: Chen pg. 246, figure 5 plurality of stress times or age times)

- relative degradation level connected between the terminals of the non-aged ("Fresh" Chen, pg. 247, figure 11) version, the magnitude of the respective quantized (age times as stated in spec. pg.6, lines 19-26: Chen pg. 246, figure 5 plurality of stress times or age times)
- current in each of the current sources determined from the aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information of component; and determining the degraded operation of the circuit by simulating

the independent current magnitudes derived from the respective aging model (Chen: pg. 244 "Model Formation" equation 1 "Age parameter") information and respective relative degradation level at the supplied circuit stress time (Chen: pg. 246, figure 5, plurality of stress times) value.

Regarding claims 91

Kadoch teaches

- the transmission to a client (Kadoch: column 2, line 6) device a program of instructions, thereby enabling the client device to perform, by means of such program,

Section II: Response to Arguments

Claim Objections

7. Applicants are thanked for addressing this issue. Objections are withdrawn.

USC 112

8. Applicants are thanked for addressing this issue. Rejection is withdrawn.

103(a)

9. Applicants are thanked for addressing this issue; however, the applicants' argument are non-persuasive in view of the prior art.

Claims 1-7

10. Applicants argues that while the Kadoch reference does discuss a single run of a simulator to cover several case, the Kadoch does not disclose anything to render as obvious to simulating a circuit for multiple stress time values in a single run to determine its degraded operation. In rebuttal, the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination. Kadoch does teach a single device however the Chan reference teaches multiple devices concerning multiple stress times (Chen: pg. 246,figure 5, plurality of stress times) with time values and aging issues of multiple circuits.

Applicants state (applicants' response, pg. 19, 1st paragraph), "To use such teachings for circuit degradation simulation of multiple times would, at best, be based on hindsight gained from the present application; which is improper". The Office refutes this argument since it's not impermissible hindsight if the motivation to combine stems from the prior art.

In regard to claim 4, applicants argue this claim is allowable based on Chen reference alleged non-teaching of "timing simulation". The Chen reference teaches a "stress time" of the circuit. If one is to simulate a circuit i.e., SPICE then it's obvious to one of ordinary skill that conducting a stress time analysis of the circuit is simulating a specific factor of the circuit.

In regard to claim 5, if one of ordinary skill is conducting a simulation of a circuit, naturally one would want to save the results of that simulation. This rebuttal is in response to arguments regarding the prior art alleged silence to the limitation of

"derived from electrical test data" to which this limitation is an intermediate step that the user performs in a circuit simulation event.

In regard to claim 7, the prior art denotes circuit speed, the aged circuit equation (Chen, pg. 244, equation 2). The equation is to find the how much time will a circuit last, thus it would be obvious to one of ordinary skill to manipulate the distance formula to produce a speed value. The rejection, as stated above, stands.

Claims 93 and 9-20

11. The "independence performance criterion for each set" limitation the applicants are arguing is a feature that is under the control of the user in which the individual has an infinite amount of scenarios. Furthermore, to repeat, the aging equation denoted in the Chen reference is suggested that each circuit is susceptible to the use of this simulation parameter.

Applicants state the Rajgopal reference is silent to the "distinct sets of components" but teaches "the system" and "components". Firstly, Rajgopal at least suggest this limitation. Secondly, "distinct sets of components" can be for example, 1k resistor as opposed to 100k resistor or analog/digital components, which is well known to one of ordinary skill in the art.

In reference to "driving capability" and "performance criterion factor", these factors are well known in the transistor art. Driving a circuit is a term for obtaining the best performance of the circuit without destroying its chemical materials. Furthermore, "different models for simulating the same type" is an intermediate step that's conducted

by the user; for example, one might simulate a pair of two stage common emitters, each having a different variable resistor. The rejection, as stated above, stands.

Claims 94 and 22-29

12. Applicants argue that the reference fails to show the use of a degradation level or its specification; however, the Office believes claim 94 in this case, is silent to this issue.

Applicants argue that the prior art fails to disclose a "first set" and a "second set" of components (i.e., claim 27, "...the first and second sets of components each consist of different device type"). In response, these devices types can be anything (i.e., transistors, capacitors, op amps, digital block (different types of digital circuits), analog block (different types of digital circuits) etc.), to which each reference mentions, or at least suggests, any one of these examples.

In reference to the "relative scale of the degradation" limitation, the Office directs its rebuttal to page 9, lines 20-26 of the disclosure,

At step 103, ***the device degradation screening means allows a user to assign different amounts, of device age****, degradation and/or lifetime for different circuit blocks, circuit block types, devices, device models, and device types in absolute or* ***relative scales****. For those devices which have pre-specified degradations, the computation of their degradations can be skipped. Relevant device characterizations (shown in step 105) can also be skipped. This will improve simulation efficiency and reduce memory usage. This step is optional.*

This paragraph defines a degradation screen process that includes "relative scales". It's apparent that Chen (pg. 243, left column, 2nd paragraph) does teach degradation process, which leaves to reason that the "relative scales" limitation engulfs this process. The rejection, as stated above, stands.

Claims 95,96 and 52-58

13. The limitations of "revising a netlist" and "plurality of independent current sources" are common integral steps of a circuit simulation software platform i.e. SPICE to which Chen makes reference to. Each time a circuit is amended a revised net list is completed. Furthermore, it's common for circuits in today's level of intricacy to have a plurality of independent current sources.

The Chen denotes a "fresh circuit". Logically, if one replaces or inserts a non-aged version then the circuit must be none other than "fresh". Furthermore, the Office finds little distinction between "degraded device characteristics" and "a distinct mechanism degradation parameter" since parameters define a characteristic of something or an event. The rejection, as stated above, stands.

Claims 97 and 61-65

14. Updating the models is an intermediate step conducted by the user. To repeat, the aging property and its relative steps are denoted by Chen as previously stated within this section of the office action. Although the Rajgopal does suggest components, the user has the ability to select any series of components.

The Chen reference does suggest gate current with its particular properties. Regarding revising of a netlist, see the rebuttal of claims 95,96 and 52-58 above.

The disclosure (page 17, lines 8-21) states the following:

Input parameters, intermediate and final results can be shared among all the user defined data, such as passing I.sub.sub to I.sub.g, as I.sub.g.varies.I.sub.sub. This can also include bias conditions, so that a function, say, age can now be a function of parameters beyond I.sub.ds, age.fwdarw.age(I.sub.ds,V.sub.ds,V.sub.gs,V.sub.bs), and so on. Multiple user defined data of the same functionality (such as the device age) can be integrated with the other user defined data. The user may have multiple equations of how, say, age model is calculated and may call any of these. Users have the flexibility to choose any one of them. User defined data can also be combined with the internal data in the hot-carrier circuit simulator (201) to fulfill the device age/degradation calculation. Again, these can be data that come with device or add in some proprietary ones the user has added in. The user defined data can be incomplete. For any of the user definable data not defined, internal data will be used. ***User defined functions can access intermediate results of circuit simulation, such as the saturation voltage, V.sub.dsat, or threshold voltage, V.sub.th, and not just I.sub.ds.***

The highlighted areas of this passage states the user has the ability to access the intermediate results, for selected components (Rajgopal) thus is an intermediate step to any circuit analysis program. The rejection, as stated above, stands.

Claims 98,76, 77

15. The updating of models or incorporation aging is suggested in the Chen reference coupled with the user's ability to update any model data, specifically model aging data. Substrate current is part of a MSOFET device, which is disclosed in Chen. Regarding revising of a netlist, see the rebuttal of claims 95,96 and 52-58 above. The rejection, as stated above, stands.

Claims 91,92,99-104 and new claims 105-110

16. Arguments to these claims are previously discussed above.

Information Disclosure Statement

17. Applicants are thanked for responding to this issue. The objection is withdrawn.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (7:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

December 4, 2006

TS

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